PRELIMINARY

DS4802
Low Voltage, Micro Power, High Performance, Rail-To-Rail Dual Op-Amp

www.dalsemi.com

FEATURES

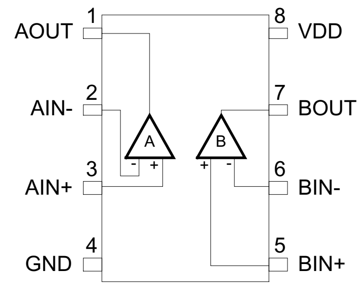
- Very low operating power: 12 µA typical per amplifier
- High output sink/source capability
- Supply Voltage Range 1.8 to 5.5V
- Rail-to-Rail Output Swing
- Input offset voltage: 0.95 mV max.

ORDERING INFORMATION

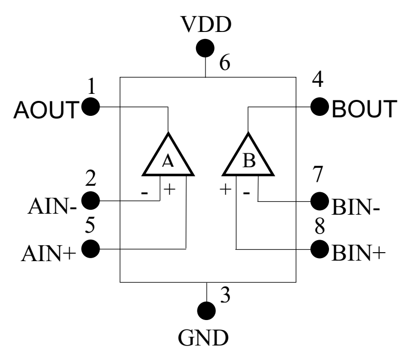
Part Number	Description
DS4802	8-pin DIP
DS4802S	8-pin SOIC
DS4802U	8-pin µ-SOP
DS4802X	8-bump Flip-Chip

For mechanical dimensions see website.

PACKAGES/PINOUTS



300-mil DIP
150-mil SOIC
118-mil µ-SOP



8-bump Flip-Chip

DESCRIPTION

The DS4802 BiCMOS dual operational amplifier combines low input offset voltage, very low power consumption, rail-to-rail output swing, and excellent DC precision. With a maximum input offset voltage of 0.95 mV, a maximum I_{DD} of 25 µA/amplifier, and 10 pA typical input bias current, the DS4802 is ideal for measurement, medical, and industrial applications. The DS4802 is also ideal for portable applications with 1.8 volt to 5.5 volt single supply voltage operation and low power consumption.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} (see Note 1)	5.5V
Differential Input Voltage (see Note 2)	$\pm V_{DD}$
Input Voltage Range, V_I (see Note 1)	-0.3V to V_{DD}
Input Current, I_{DD}	± 4 mA
Output Current, I_O	± 50 mA
Total current into V_{DD}	± 50 mA
Total current out of GND	± 50 mA
Duration of short-circuit current (See Note 3)	unlimited
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

Notes:

1. Relative to GND.
2. Non-inverting input relative to inverting input. Excessive current flows when input is brought below GND - 0.3V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD}	1.8		5.5	V	1
Input Voltage Range	V_I	GND		V_{DD} - 1.0	V	1
Common-Mode Input Voltage	V_{IC}	GND		V_{DD} - 1.0	V	
Free-Air Operating Temperature	T_A	0		70	°C	

Notes:

1. Voltage referenced to GND.

ELECTRICAL CHARACTERISTICS (TA: 0°C – 70°C. VDD = 1.8V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Offset Voltage (V_{IC} = 0.5V, R_S = 50Ω, V_{OUT} = V_{DD}/2)	V_{IO}		0.1	0.95	mV	
Temperature Coefficient of Input Offset Voltage (V_{IC} = 0.5V, R_S = 50Ω, V_{OUT} = V_{DD}/2)	αV_{IO}		2		μV/°C	
Input Offset Current (R_S = 50Ω)	I_{IO}		5	500	pA	
Input Bias Current (R_S = 50Ω)	I_{IB}		10	500	pA	
Common-mode Input Voltage Range (|VIO| ≤ 5 mV, R_S = 50Ω)	V_{ICR}	0 to 1	-0.3 to 1.2		V	
High Level Output Voltage (I_{OH} = -50 μA) (I_{OH} = -500 μA)	V_{OH}	 1.5	 1.785 1.65		V	
Low Level Output Voltage (I_{OL} = 50 μA) (I_{OL} = 500 μA)	V_{OL}		 10 100	 200	mV	
Large Signal Differential Voltage Amplification (V_{IC} = 0.5V, 0.4V ≤ V_O ≤ 1.4V) R_L = 100 kΩ (V_{IC} = 0.5V, 0.4V ≤ V_O ≤ 1.4V) R_L = 10 kΩ	A_{VD}	65 55	75 65		dB	
Input Resistance	R_{IN}		$>10^{12}$		Ω	
Common Mode Input Capacitance	$c_{i(c)}$		24.0		pF	
Common Mode Rejection Ratio (0V ≤ V_{IC} ≤ 0.8V, R_S = 50Ω, V_O = V_{DD}/2)	CMRR	60	75		dB	
Supply Voltage Rejection Ratio (1.8V ≤ V_{DD} ≤ 3.6V, V_{IC} = V_{DD}/2, no load)	k_{SVR}	70	85		dB	
Amplifier Supply Current (per channel) (V_O = V_{DD}/2, no load)	I_{DD}		12	25	μA	
Slew Rate at Unity Gain (R_L = 100 kΩ, C_L = 100 pF tied to V_{DD}/2)	SR	10	15		V/ms	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Equivalent Input Noise Voltage (f = 10 Hz) (f = 1 kHz)	V_N		120 60		nV/√Hz	
Unity Gain Bandwidth Product (R_L = 100 kΩ, C_L = 100 pF tied to $V_{DD}/2$)	UGBW		31		kHz	
Phase Margin at Unity Gain (R_L = 100 kΩ, C_L = 100 pF tied to $V_{DD}/2$)	ϕ_M		60		Degree	
Gain Margin (R_L = 100 kΩ, C_L = 100 pF tied to $V_{DD}/2$)			17		dB	

ELECTRICAL CHARACTERISTICS cont. (T_A: 0°C – 70°C. V_{DD} = 3.0V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Offset Voltage (V_{IC} = 1.5V, R_S = 50Ω, $V_{OUT} = V_{DD}/2$)	V_{IO}		0.1	0.95	mV	
Temperature Coefficient of Input Offset Voltage (V_{IC} = 1.5V, R_S = 50Ω, $V_{OUT} = V_{DD}/2$)	αV_{IO}		2		µV/°C	
Input Offset Current (R_S = 50Ω)	I_{IO}		5	500	pA	
Input Bias Current (R_S = 50Ω)	I_{IB}		10	500	pA	
Common-mode Input Voltage Range (|VIO| ≤ 5 mV, R_S = 50Ω)	V_{ICR}	0 to 2	-0.3 to 2.2		V	
High Level Output Voltage (I_{OH} = -200 µA) (I_{OH} = -2 mA)	V_{OH}	 2.4	 2.97 2.7		V	
Low Level Output Voltage (V_{IC} = 1.5V, I_{OL} = 200 µA) (V_{IC} = 1.5V, I_{OL} = 2 mA)	V_{OL}		 24 240	 500	mV	
Large Signal Differential Voltage Amplification (V_{IC} = 1.5V, 0.5V ≤ V_O ≤ 2.5V) R_L = 100 kΩ (V_{IC} = 1.5V, 0.5V ≤ V_O ≤ 2.5V) R_L = 10kΩ	A_{VD}	70 60	80 70		dB	
Input Resistance	R_{IN}		$>10^{12}$		Ω	
Common Mode Input Capacitance	$c_{I(c)}$		24.0		pF	
Common Mode Rejection Ratio	CMRR	65	80		dB	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
($0V \le V_{IC} \le 2V$, $R_S = 50\Omega$, $V_O = V_{DD}/2$)						
Supply Voltage Rejection Ratio ($1.8V \le V_{DD} \le 3.6V$, $V_{IC} = V_{DD}/2$, no load)	k_{SVR}	70	85		dB	
Amplifier Supply Current (per channel) ($V_O = V_{DD}/2$, no load)	I_{DD}		12	25	µA	
Slew Rate at Unity Gain (R_L = 100 kΩ, C_L = 100 pF tied to $V_{DD}/2$)	SR	10	15		V/ms	
Equivalent Input Noise Voltage (f = 10 Hz) (f = 1 kHz)	V_N		120 60		nV/√Hz	
Unity Gain Bandwidth Product (R_L = 100 kΩ, C_L = 100 pF tied to $V_{DD}/2$)	UGBW		35		kHz	
Phase Margin at Unity Gain (R_L = 100 kΩ, C_L = 100 pF tied to $V_{DD}/2$)	ϕ_M		60		Degree	
Gain Margin (R_L = 100 kΩ, C_L = 100 pF tied to $V_{DD}/2$)			17		dB	

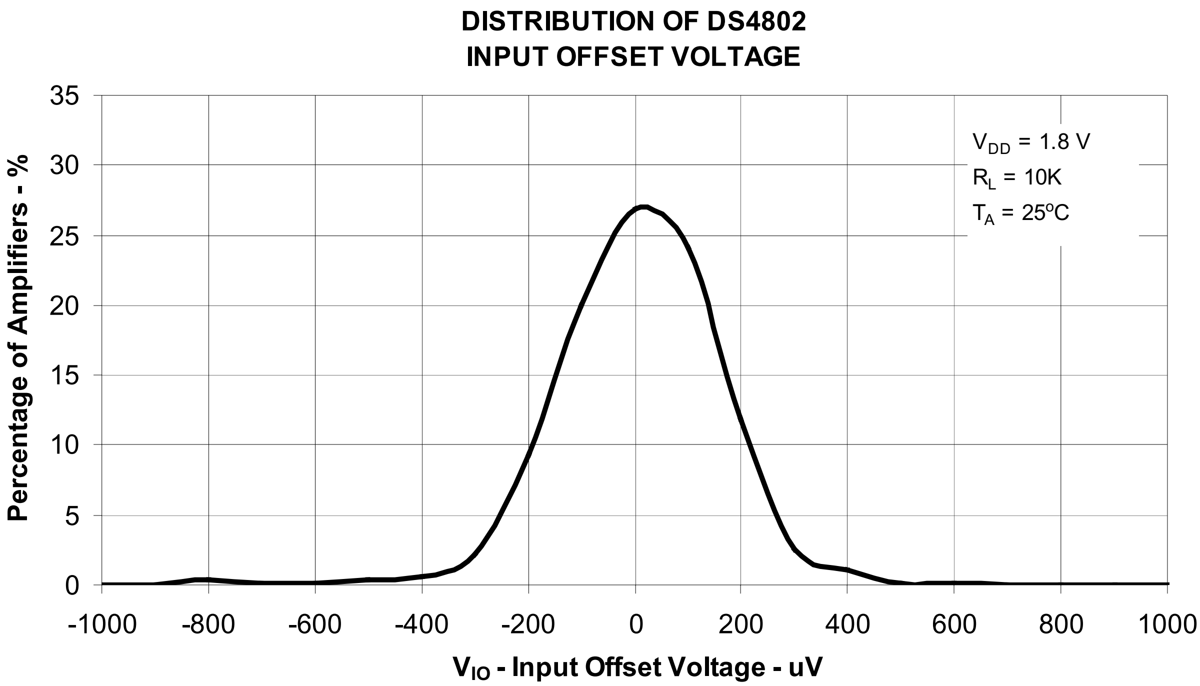


Figure 1.0

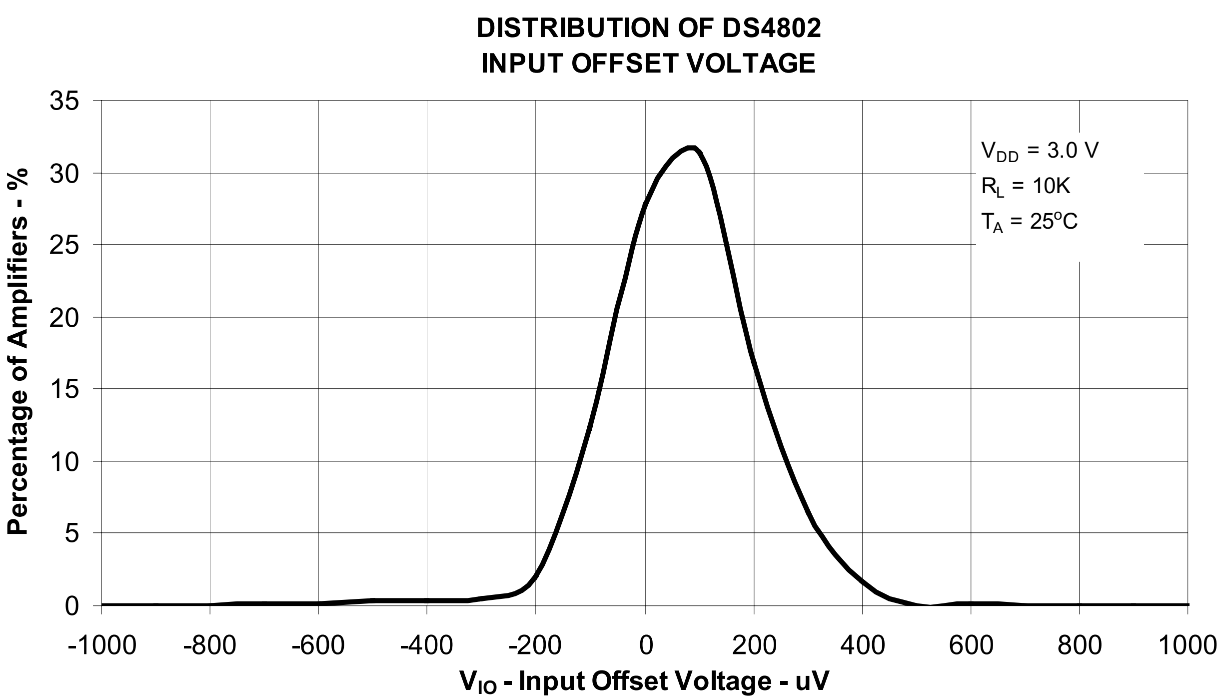


Figure 2.0

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

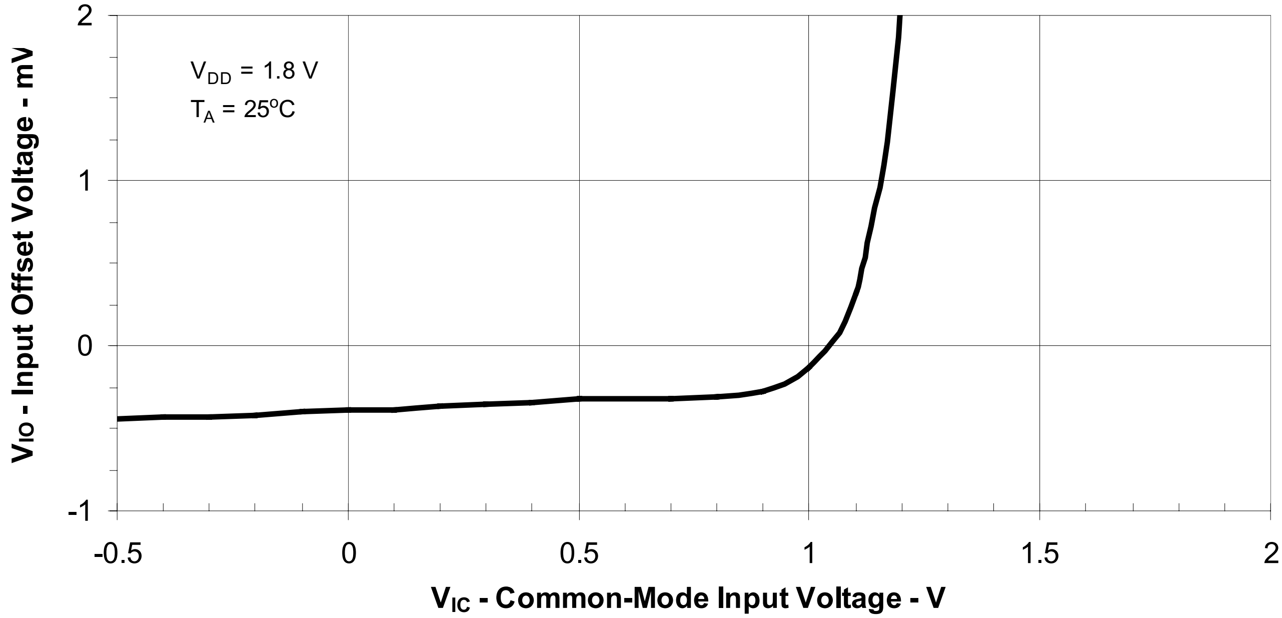


Figure 3.0

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

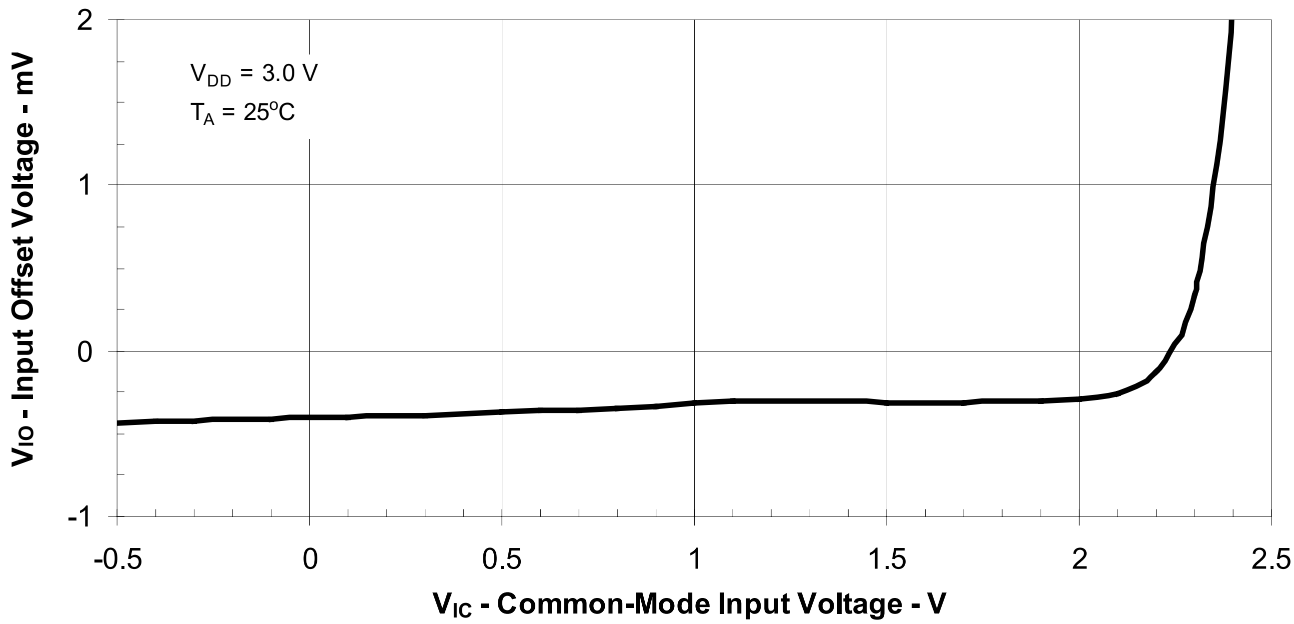


Figure 4.0

DISTRIBUTION OF DS4802
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

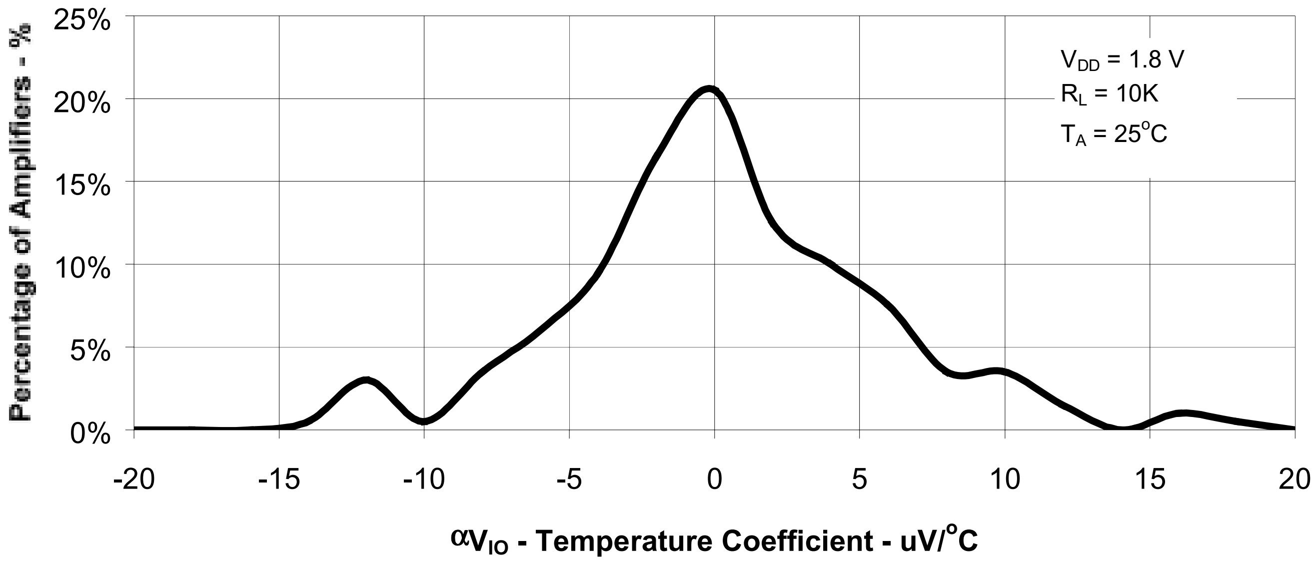
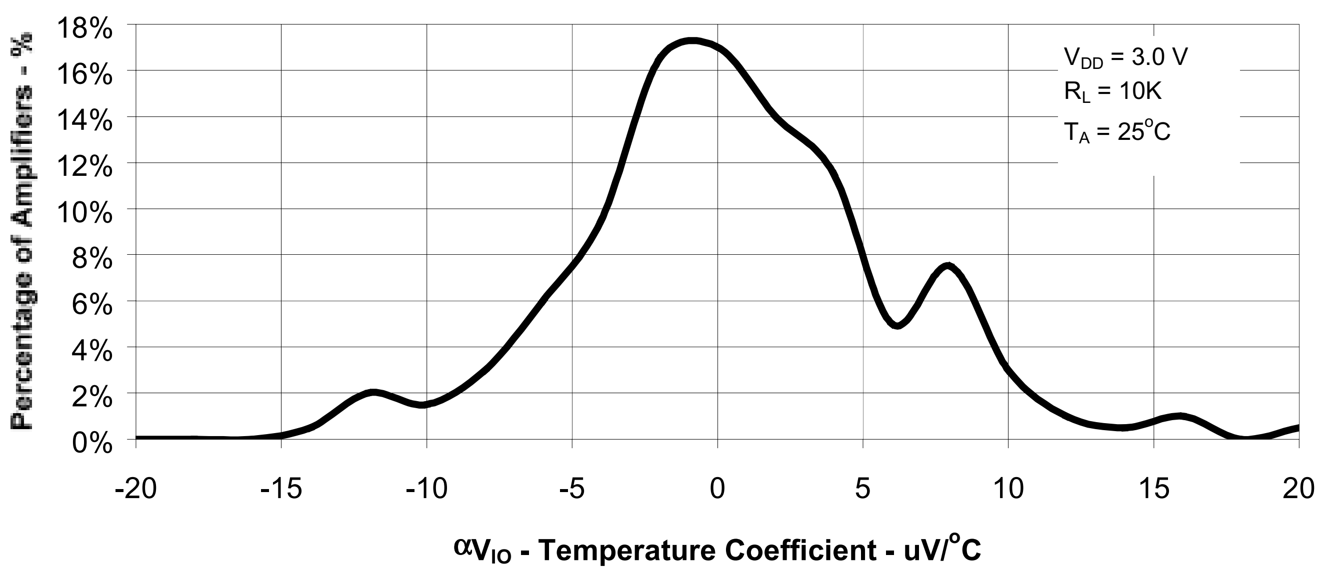


Figure 5.0

DISTRIBUTION OF DS4802
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT



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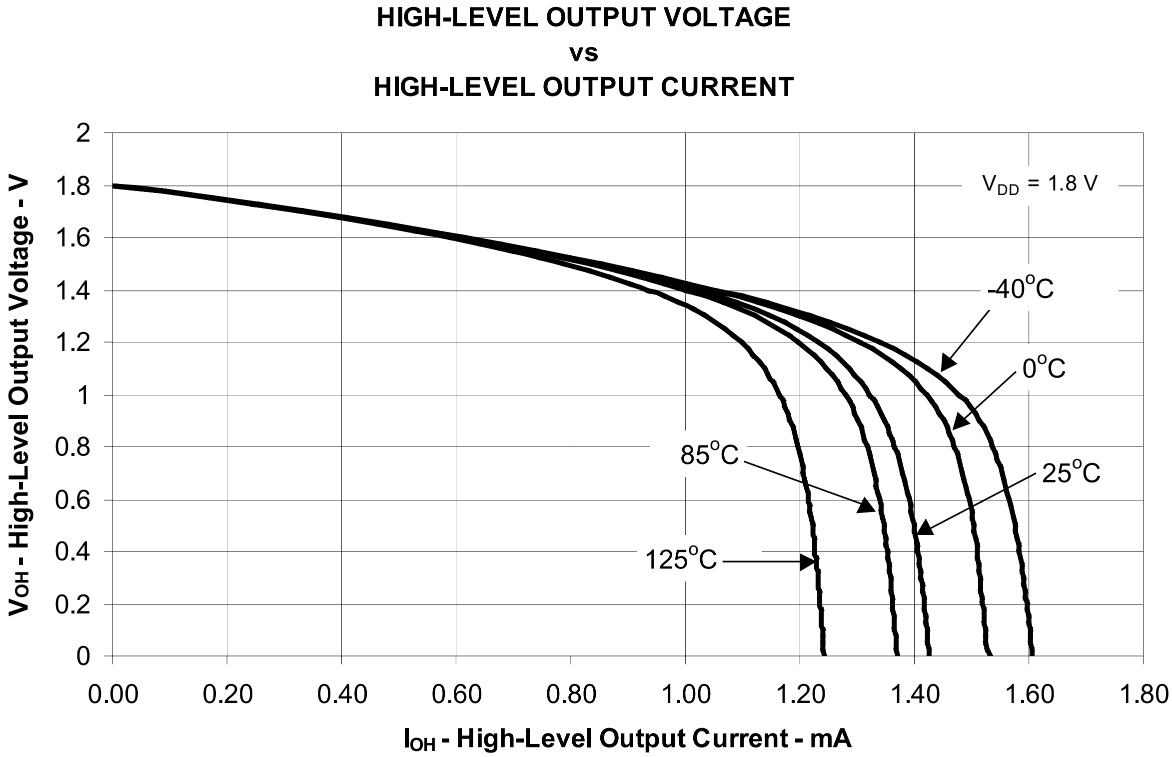

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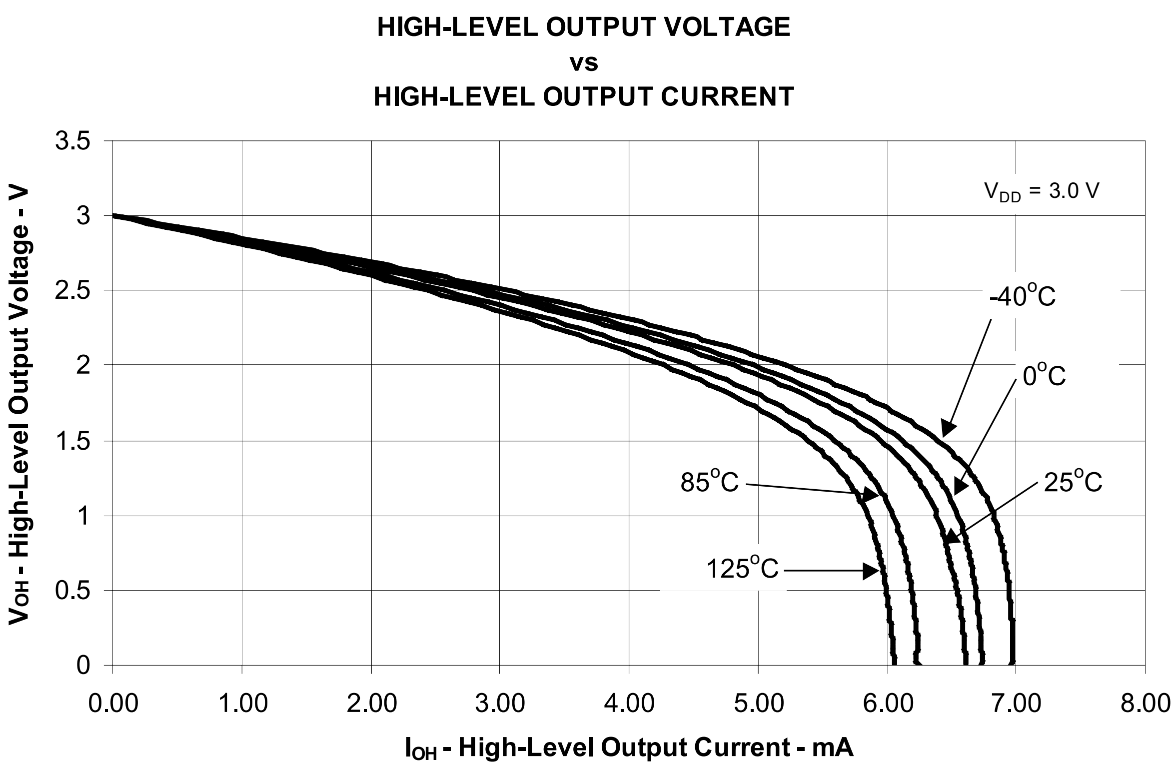


Figure 8.0

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

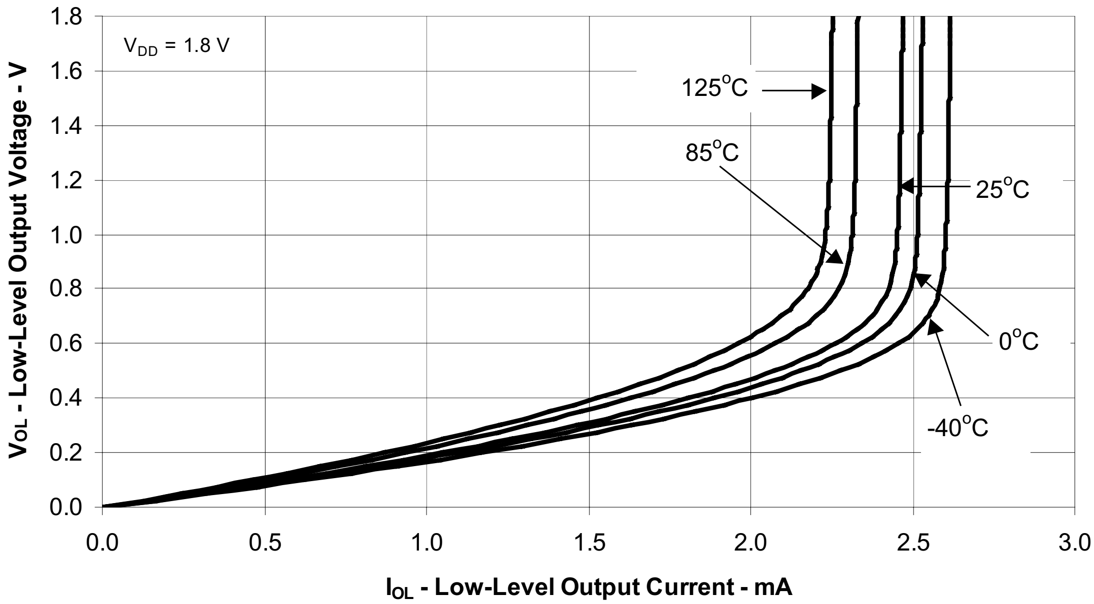


Figure 9.0

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

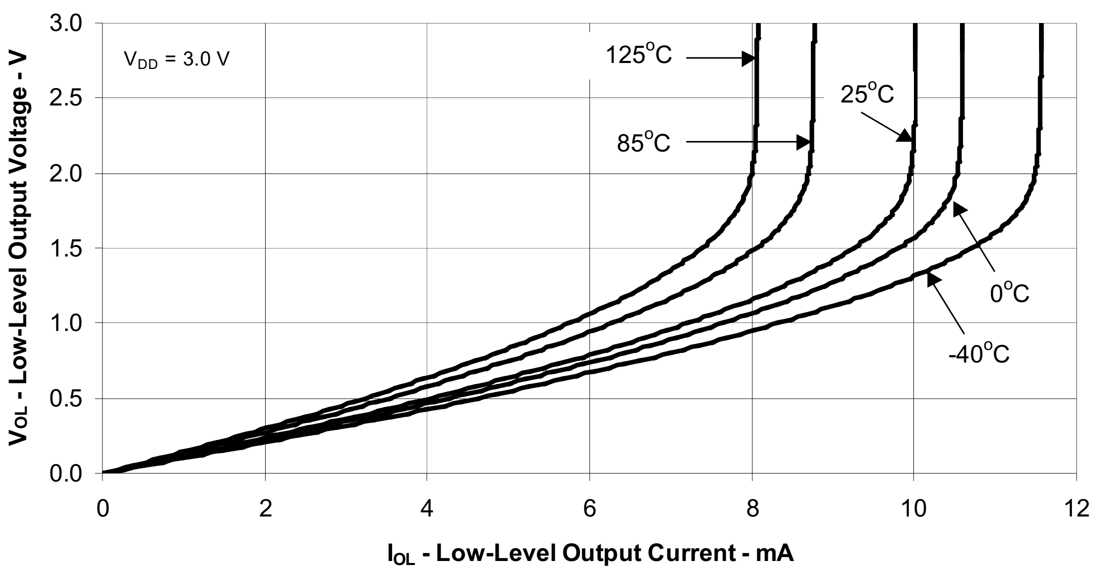
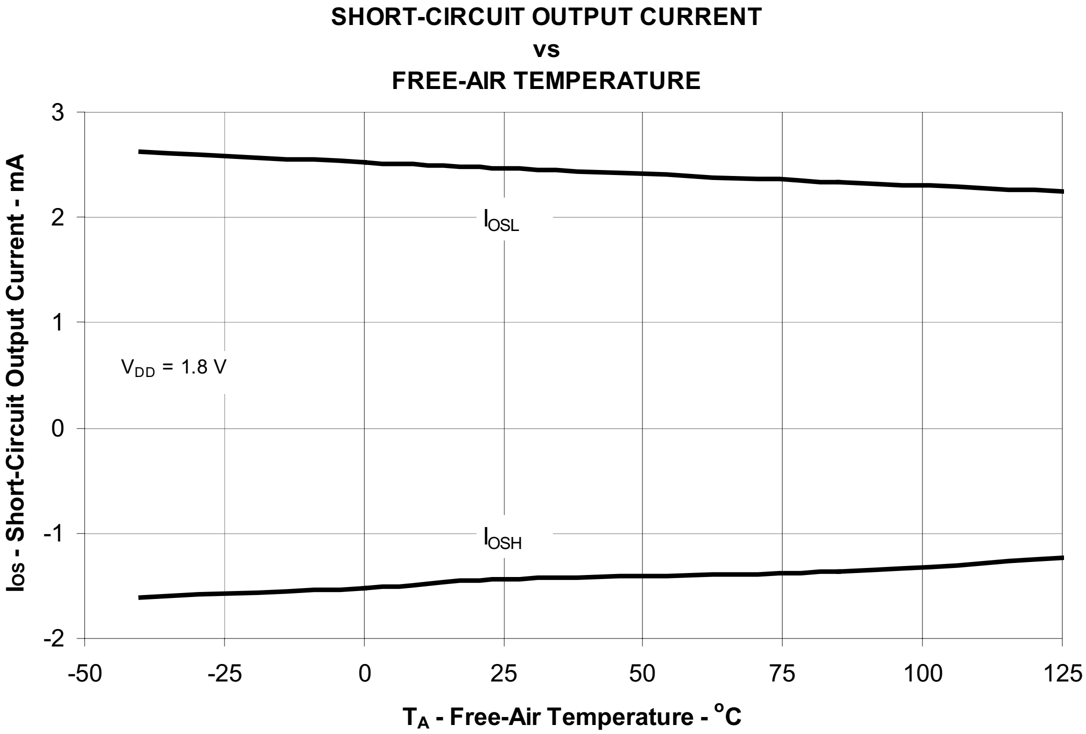


Figure 10.0



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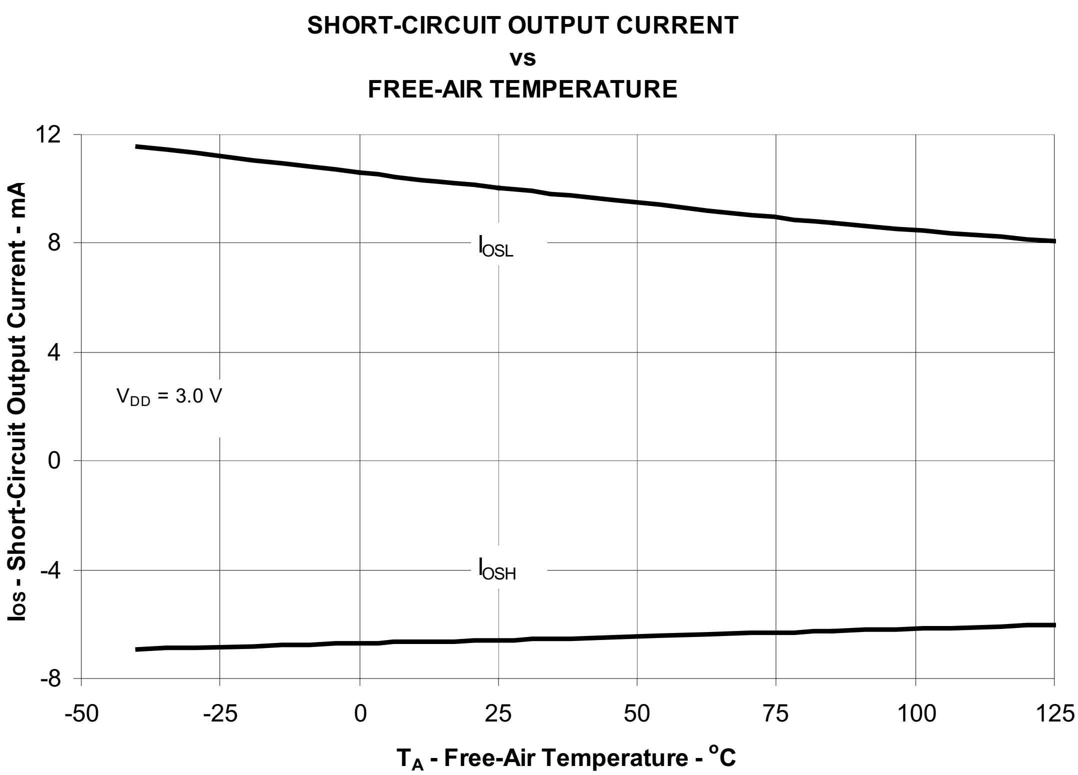


Figure 12.0

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE MARGIN
vs
FREQUENCY

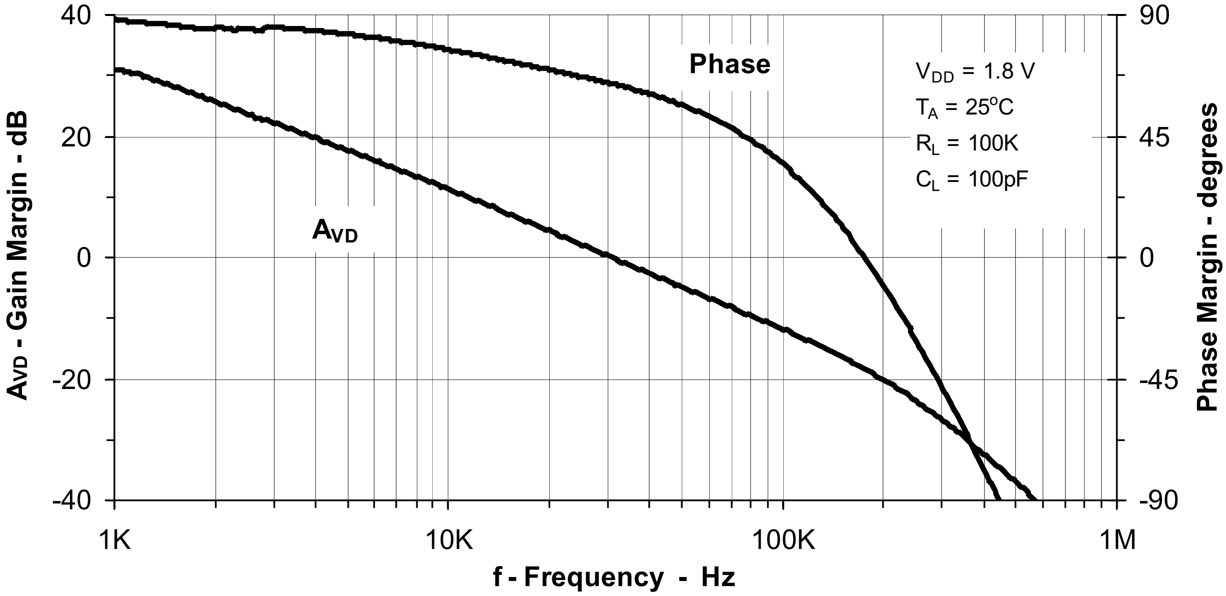


Figure 13.0

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE MARGIN
vs
FREQUENCY

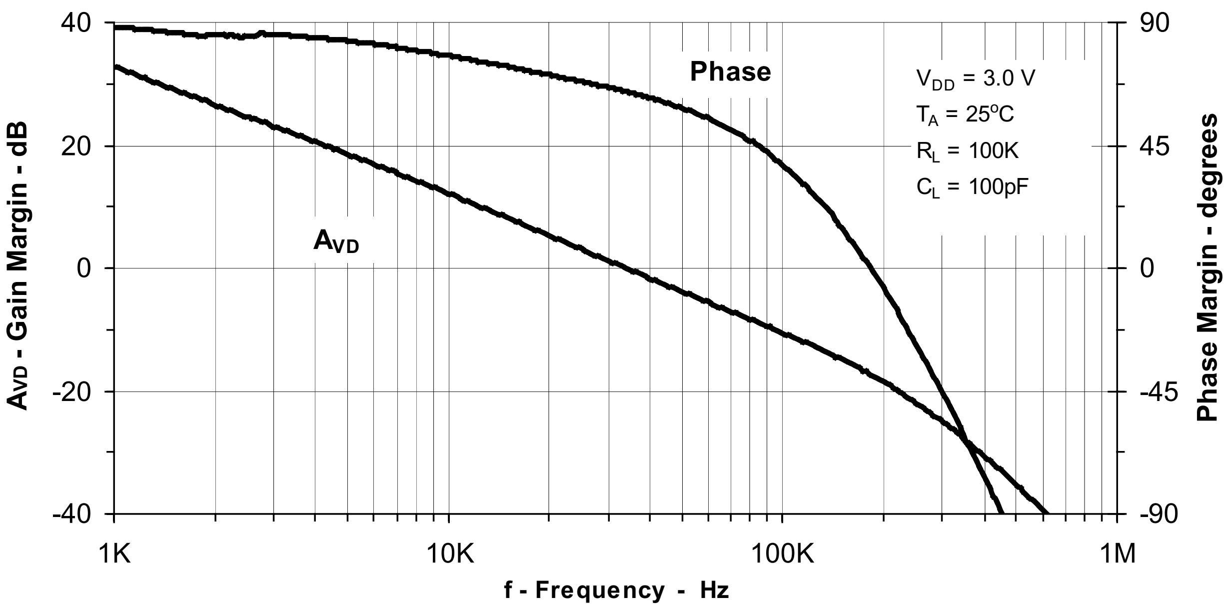
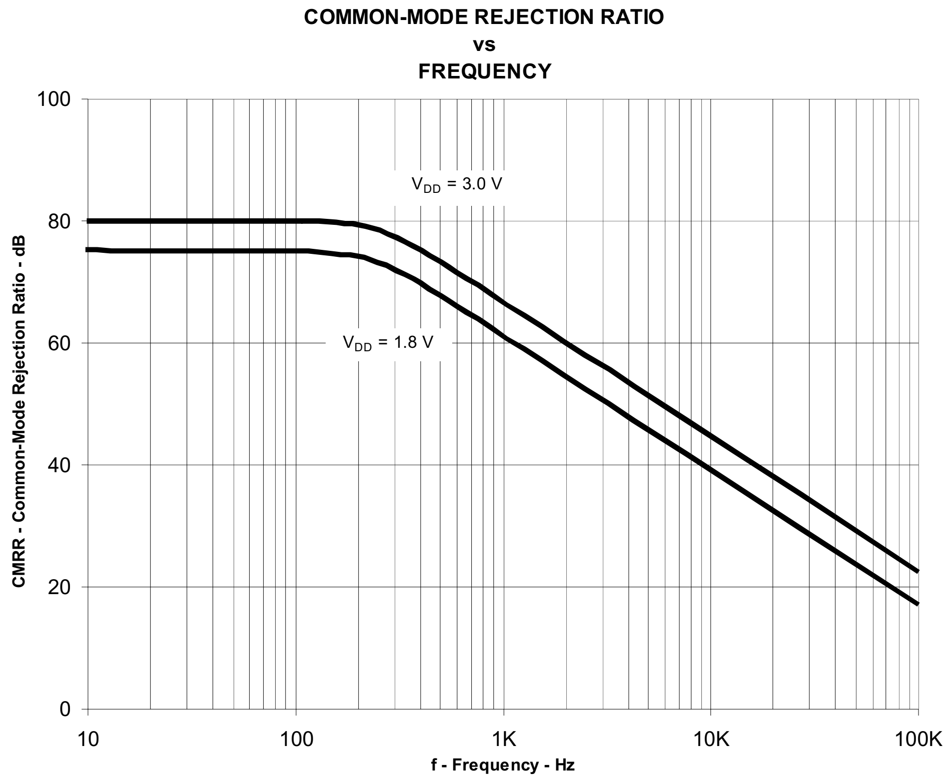


Figure 14.0



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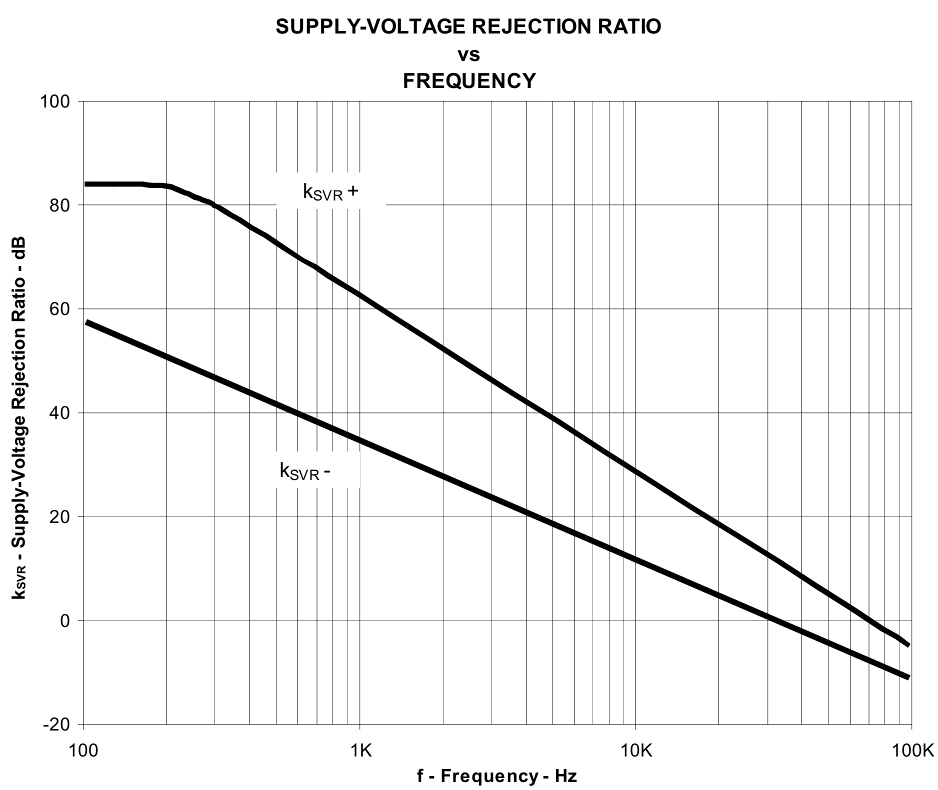


Figure 16.0

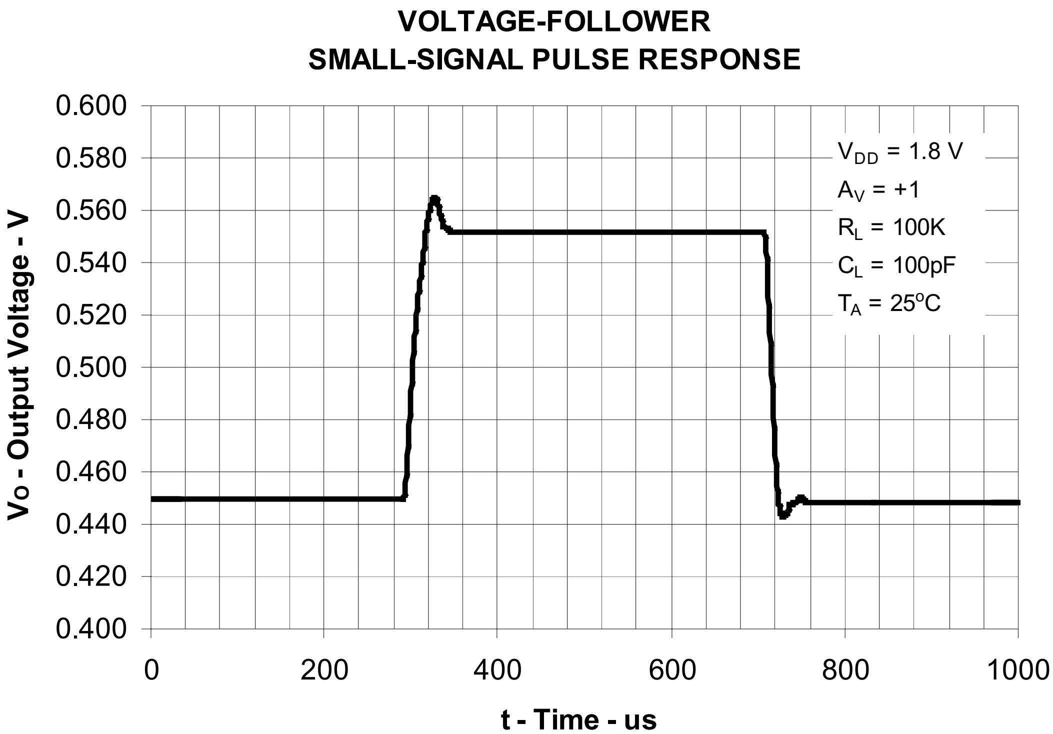


Figure 17.0

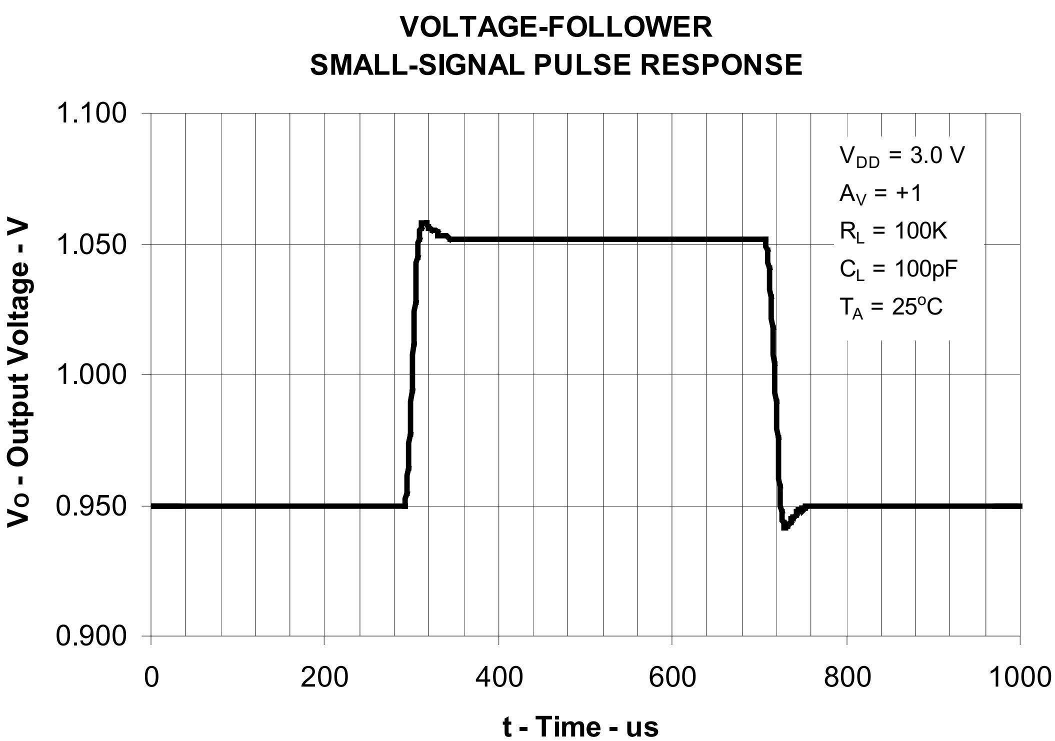


Figure 18.0

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

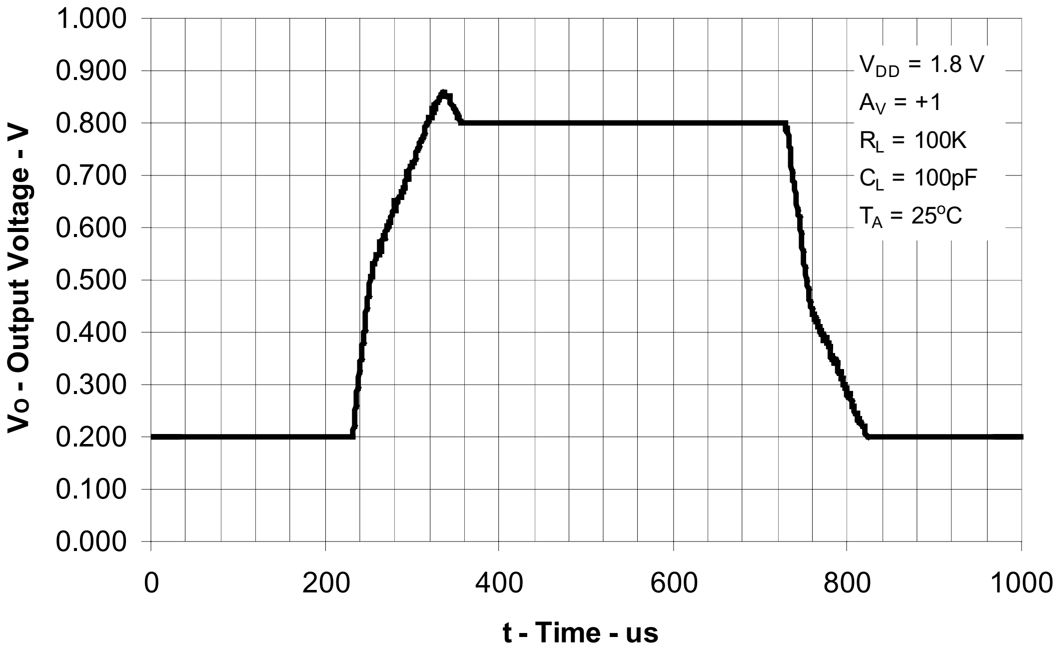


Figure 19.0

VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE

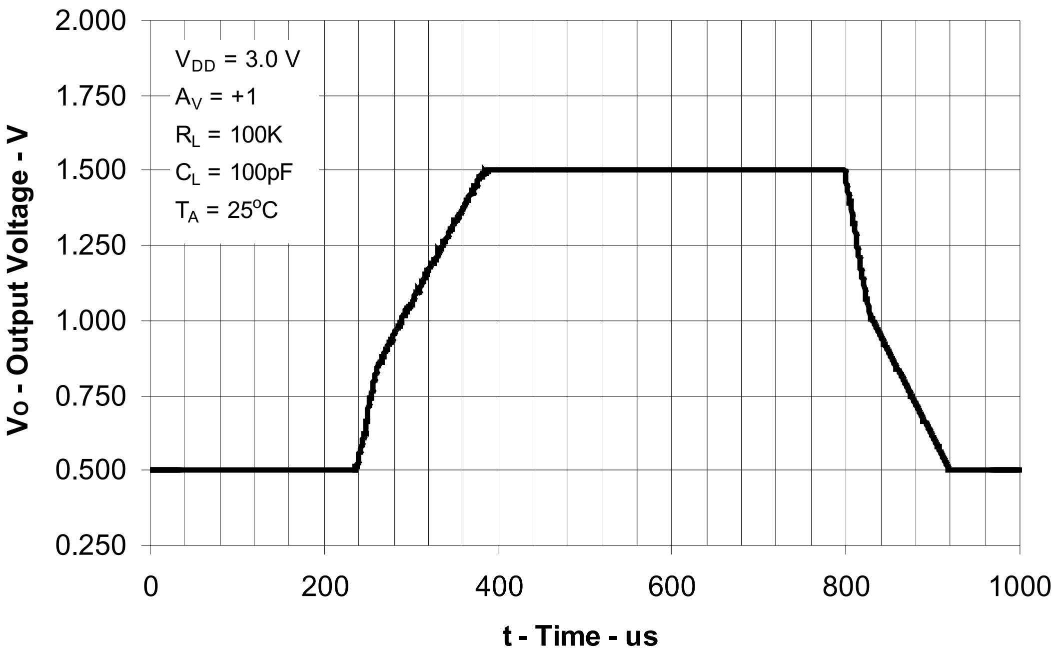


Figure 20.0

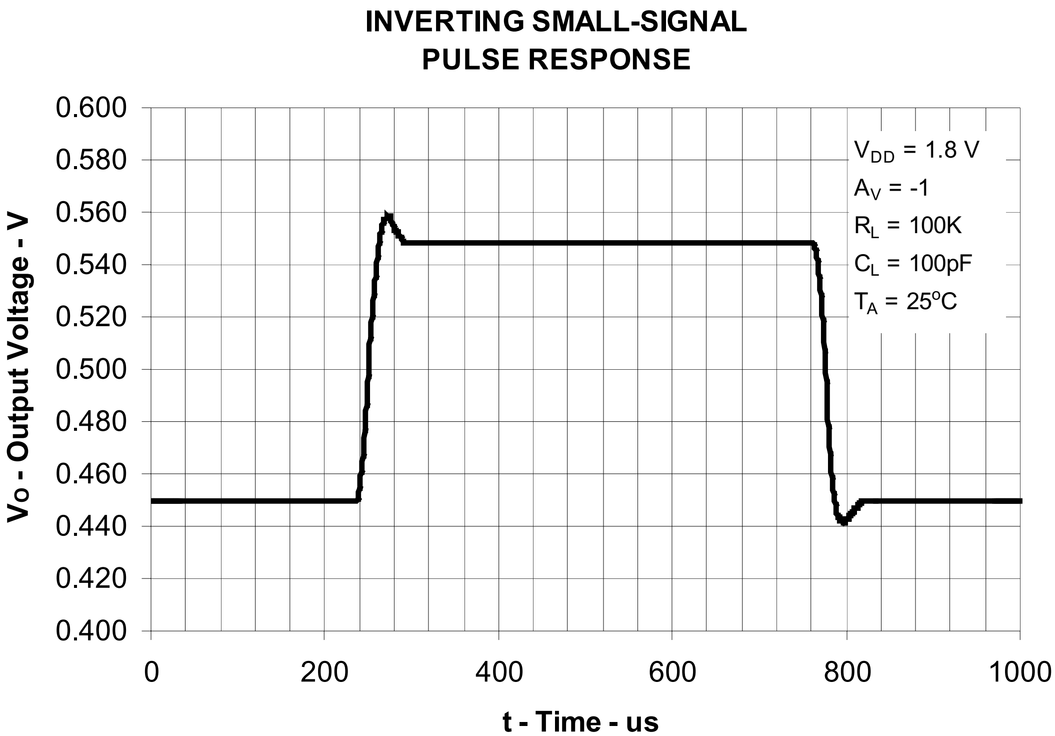


Figure 21.0

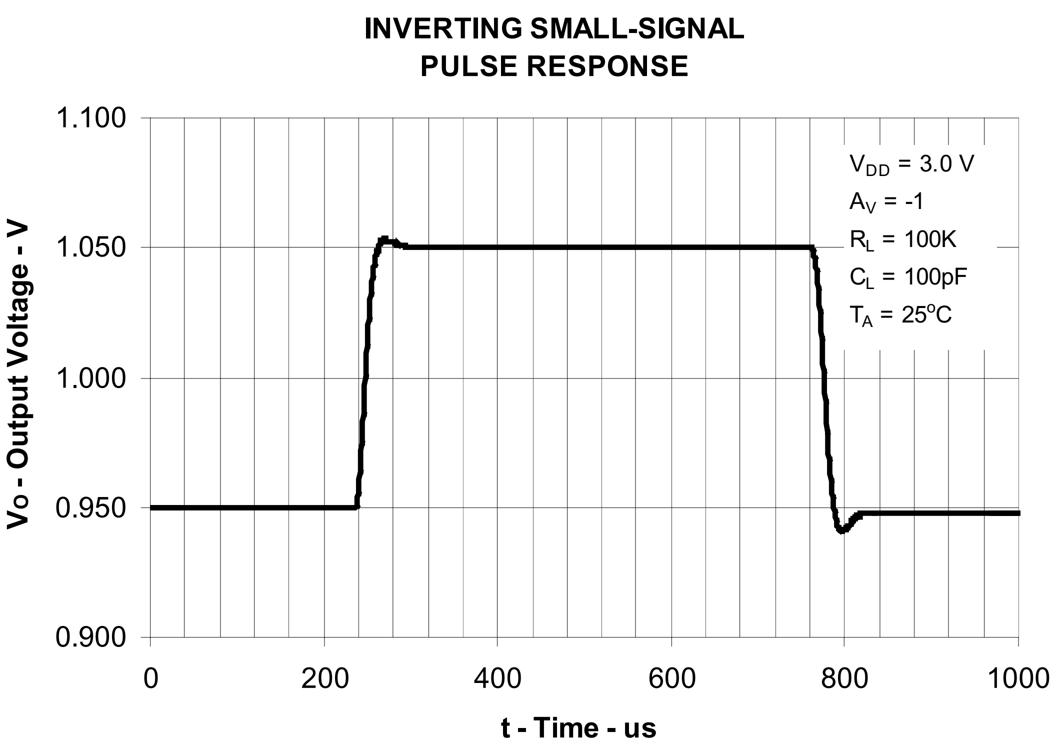
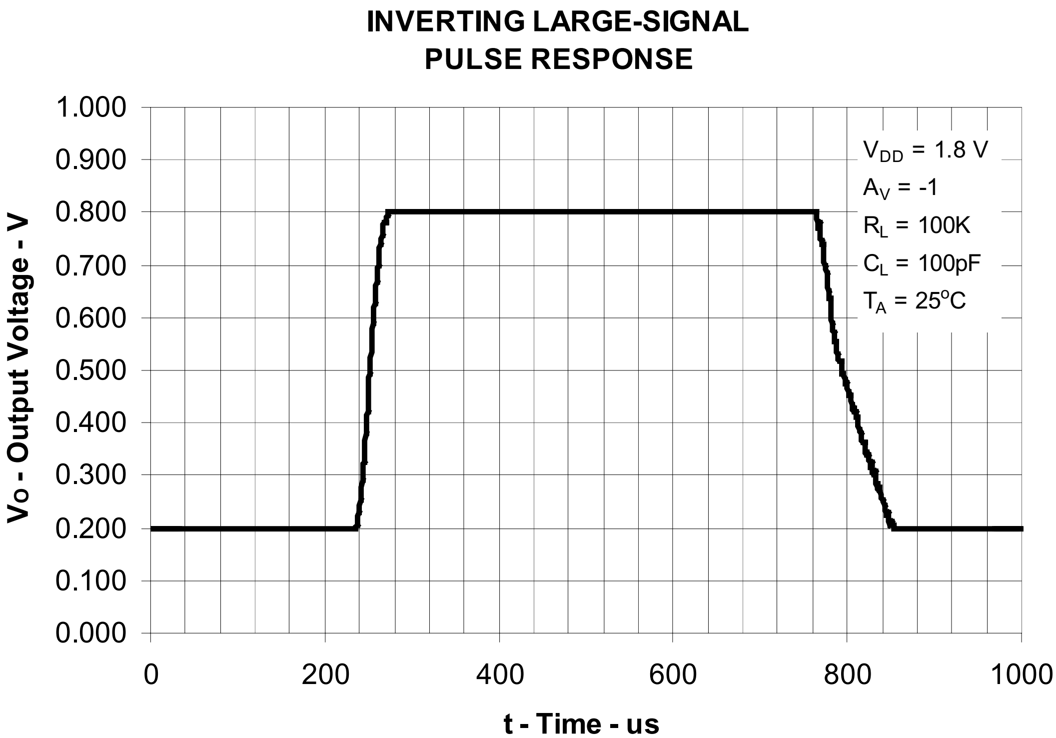


Figure 22.0



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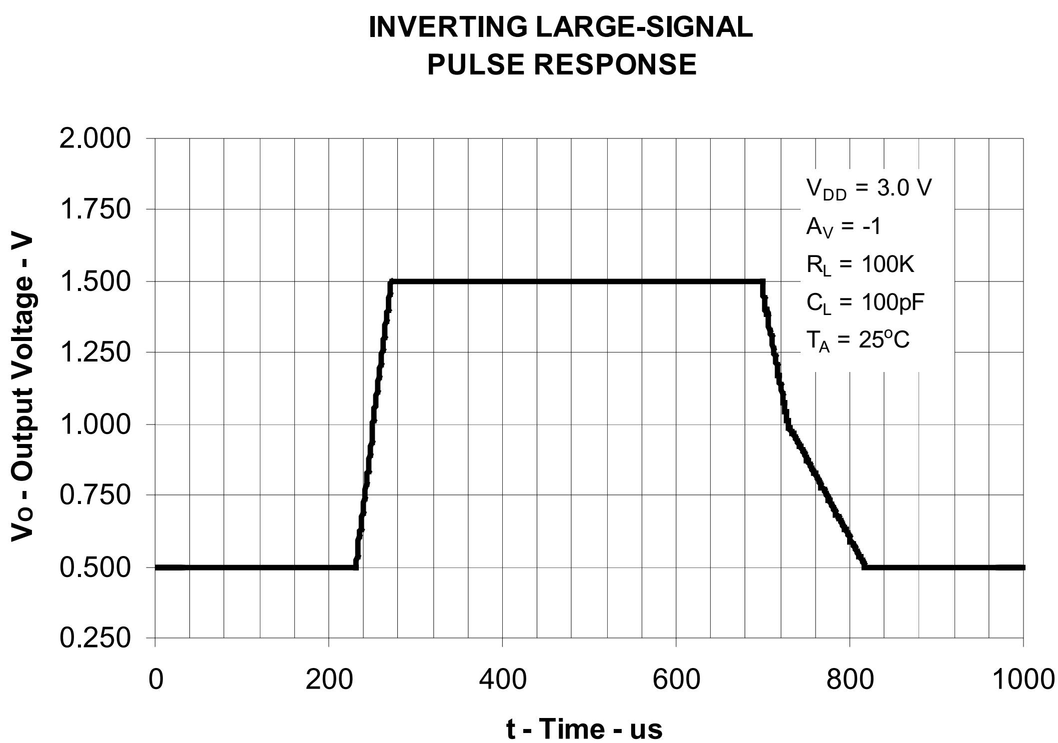

Figure 24.0

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

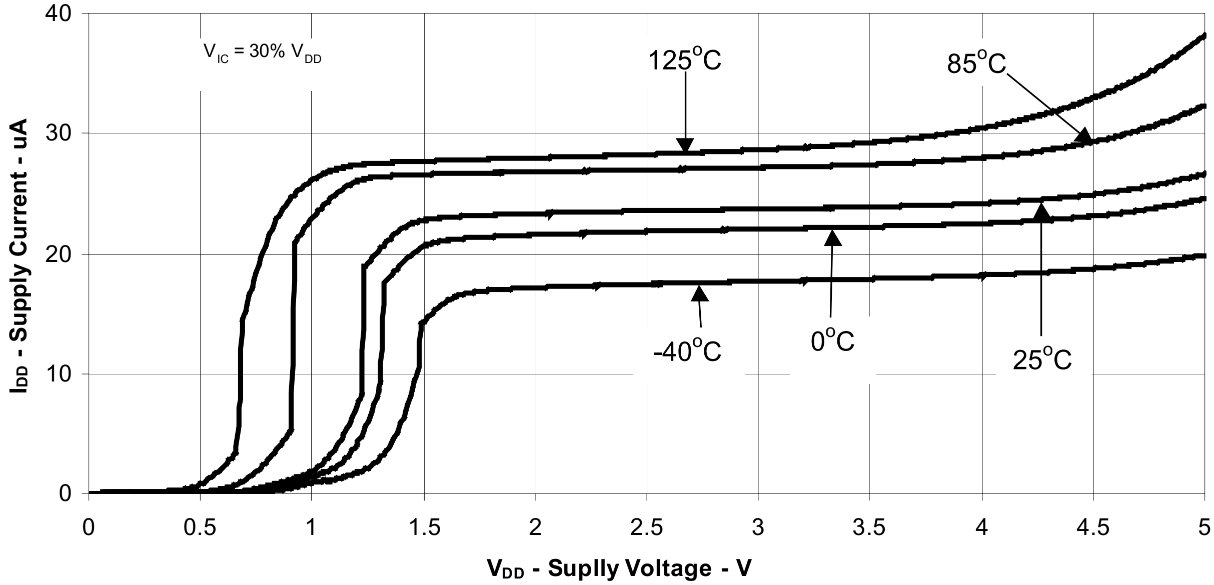

Figure 25.0

UNITY-GAIN BANDWIDTH
vs
LOAD CAPACITANCE

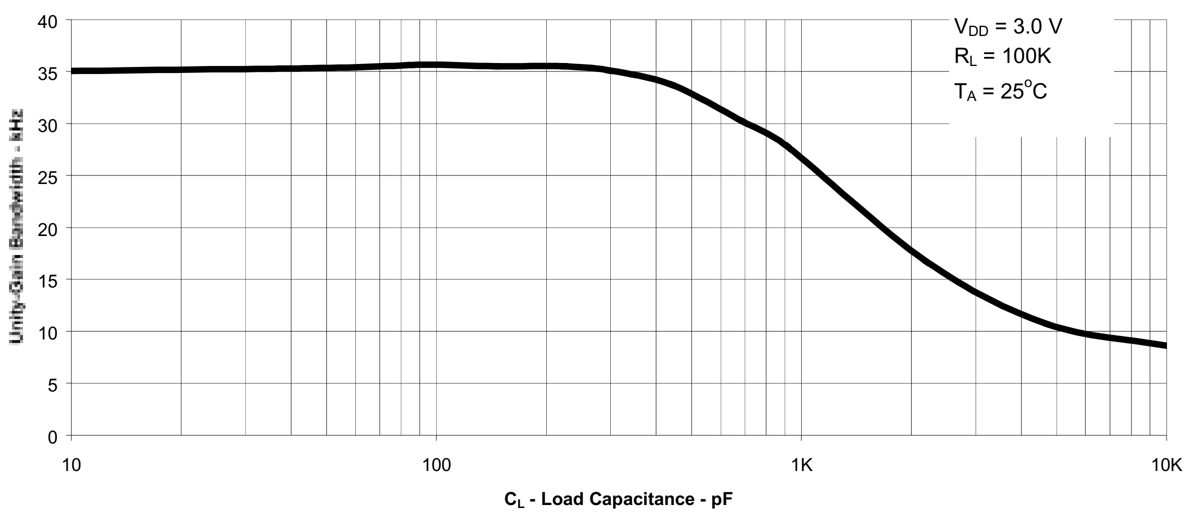

Figure 26.0

PHASE MARGIN vs LOAD CAPACITANCE

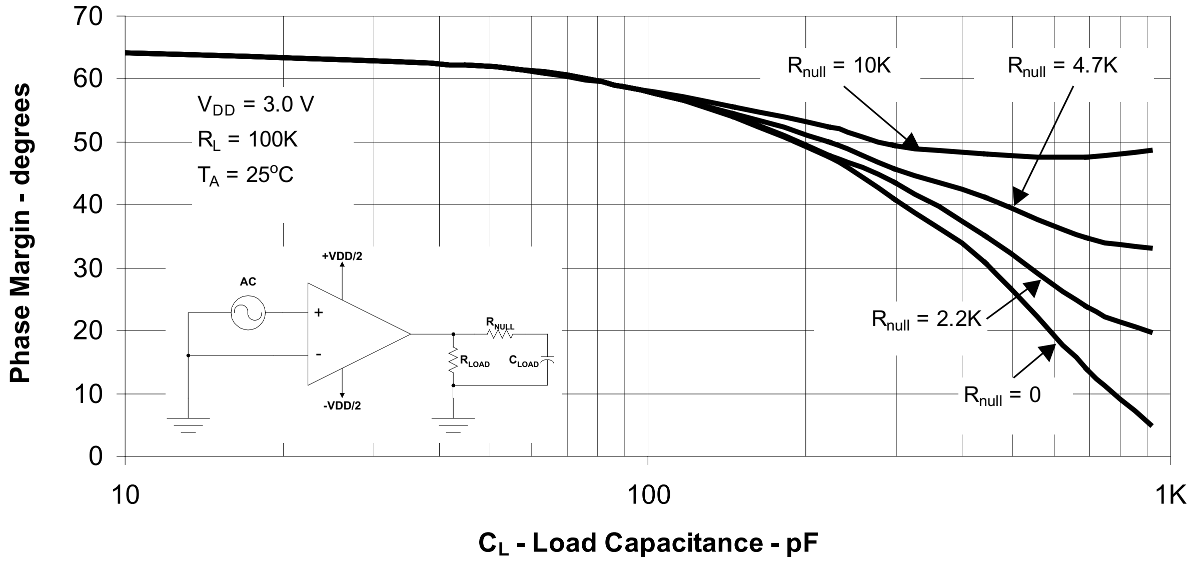

Figure 27.0

GAIN MARGIN vs LOAD CAPACITANCE

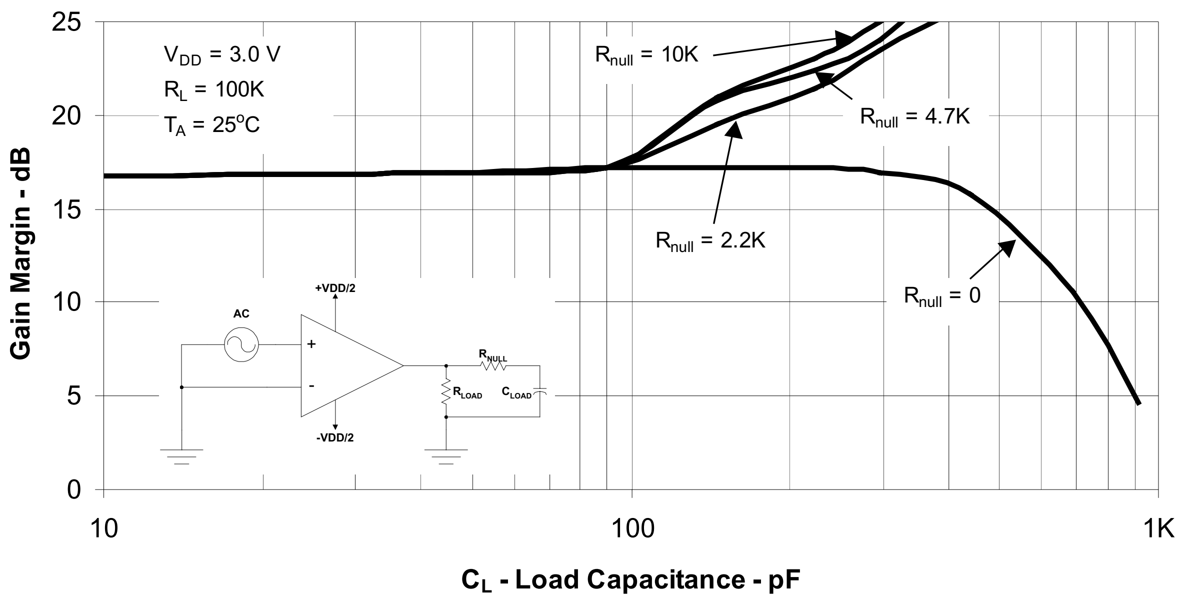

Figure 28.0